VERIFICATION OF A 65NM CMOS IC FOR VARIOUS APPLICATIONS (NEUTRINO DETECTION, HIGH ENERGY PHYSICS, ETC.)

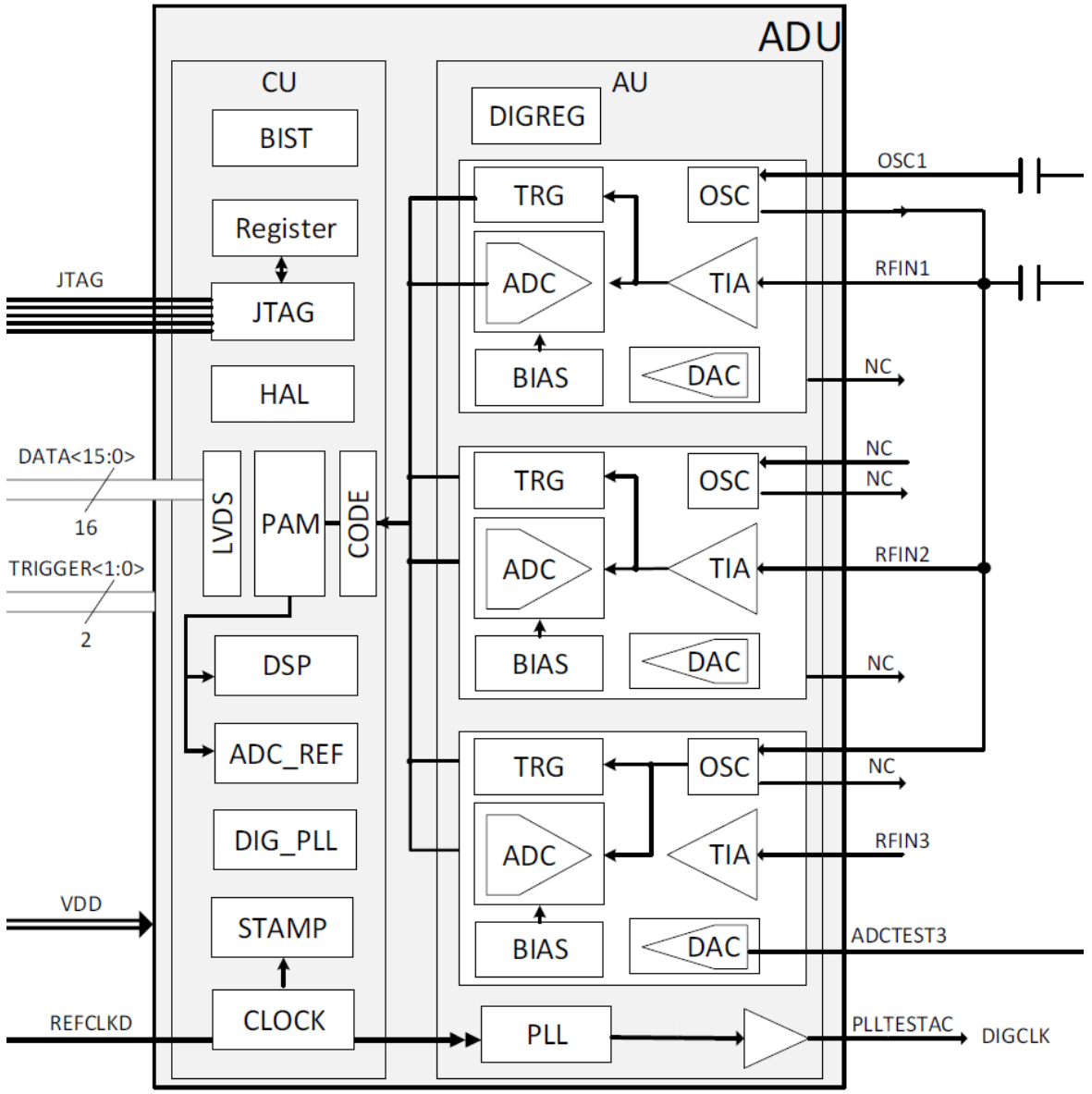
18TH APRIL 2018 I CHRISTIAN ROTH

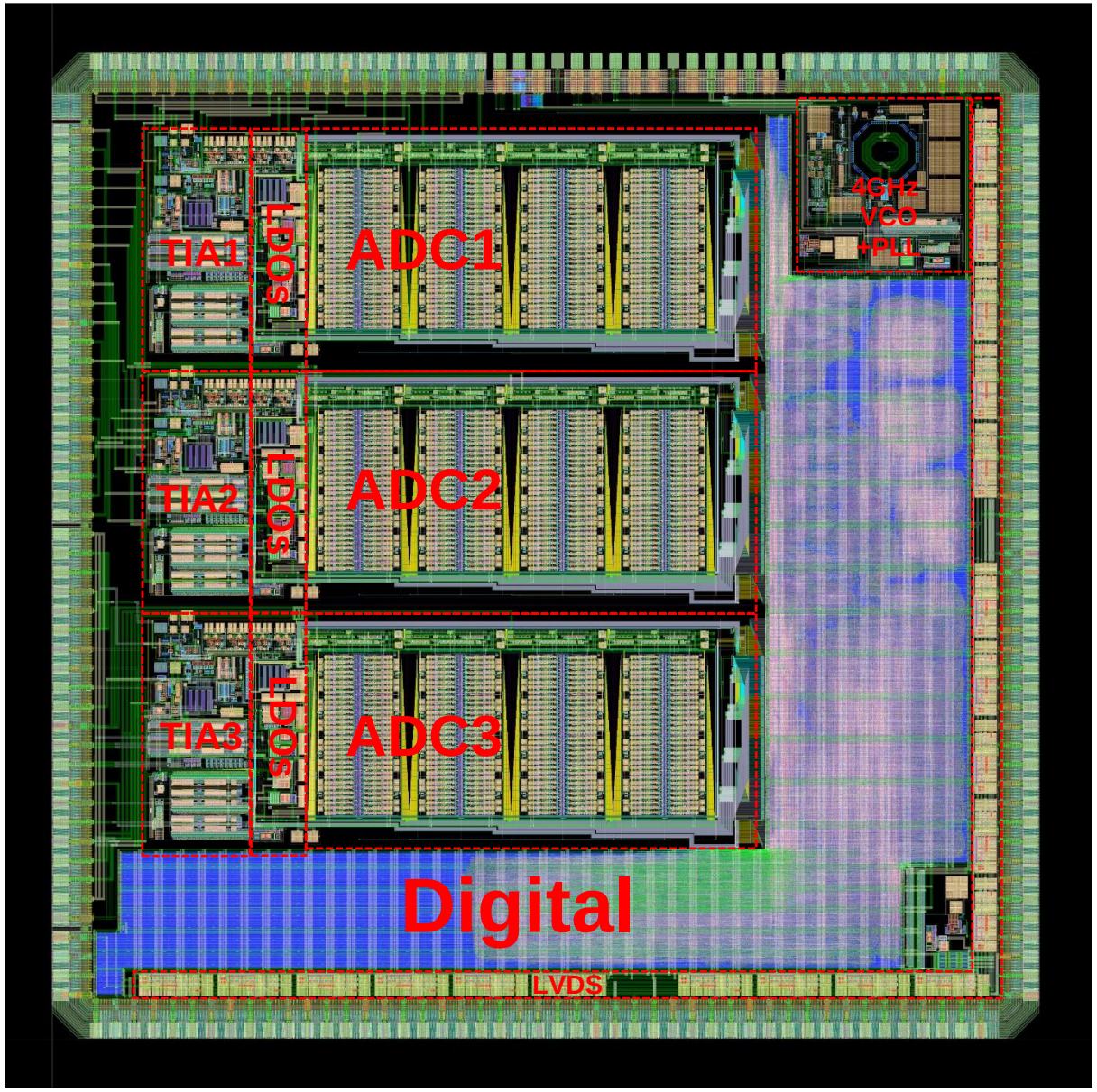
Mitglied der Helmholtz-Gemeinschaft

JÜLICH
Forschungszentrum

VULCAN CHIP OVERVIEW

- The Vulcan Chip
  - Highly linear, fully integrated circuit – **Vulcan**
    - Sampling ADC with approx. 80 dB linearity
      (3 signal chains with 3 different gains)
    - No external components required
    - On-chip clock generation from ref. clock
  - Precise signal reconstruction
    - No analog delay line
      (reducing noise & distortion)
    - Control loop to suppress DC variations
    - Optional overshoot compensation
  - Further key parameters of Vulcan:
    - ADC with 9.5 bit (3x 8 bit), 1 Gsample/s
    - Transimpedance Amplifier (TIA)
      Input impedance of < 10 Ohm
    - Power consumption ~ 1.2 Watt



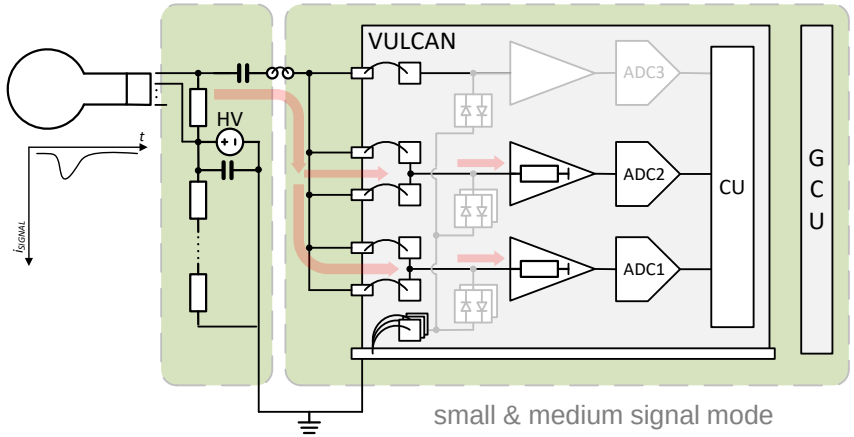


VULCAN
IC LAYOUT

Key Parameter of Vulcan	
Process	65 nm CMOS
Active Area	22 mm^2
Power	~ 1.2 W
Input Impedance	< 10 Ohm
Input Bandwidth	500 MHz
Sampling Rate	1 Gsample/s
Dynamic Range	80 dB
ADC Resolution	3x 8 bit
High Gain	0.06 p.e./bit
Medium Gain	0.4 p.e./bit
Low Gain	8 p.e./bit

VULCAN SIGNAL MODES

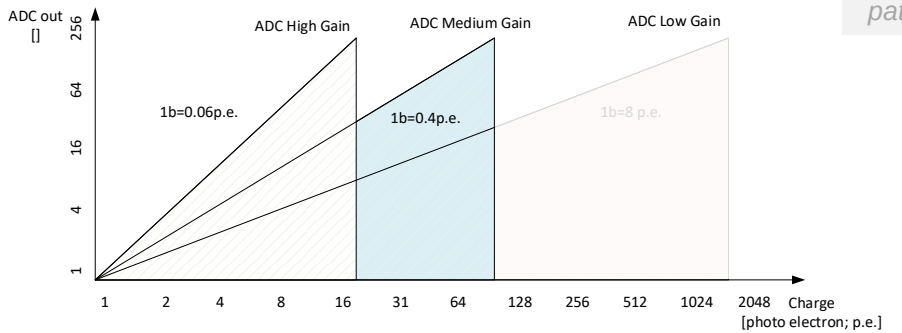
- Signal Modes – Small & Medium Signals



patent pending

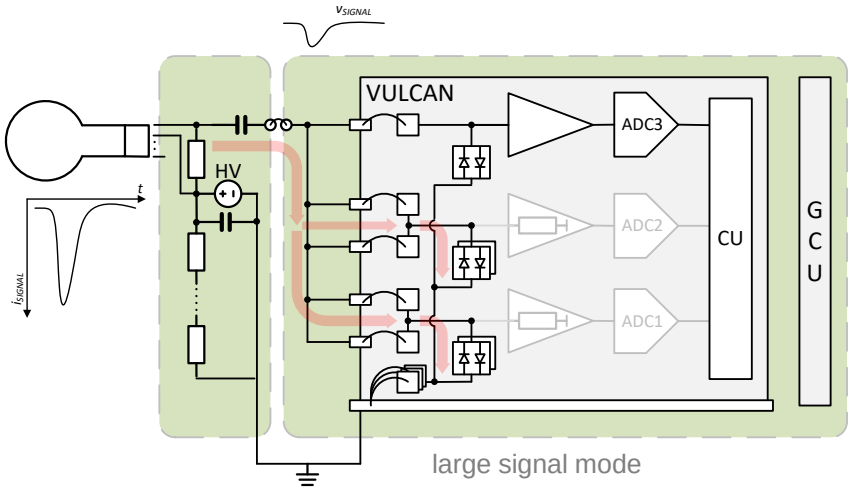
First two signal chains

- Parallel TIA input
- Programmable gains
- Combined input resistance $R \approx 5\ \Omega$



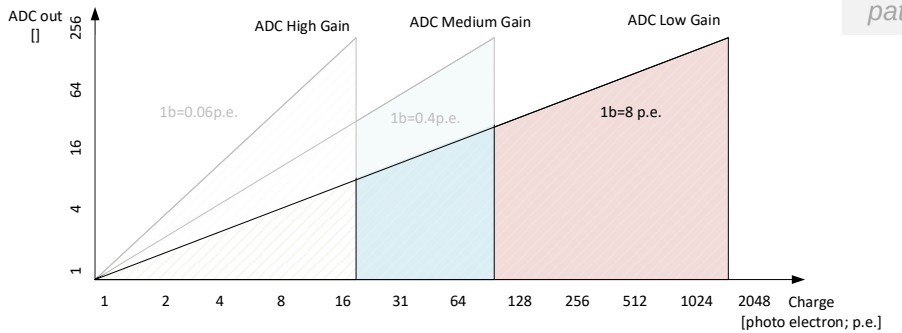
VULCAN SIGNAL MODES

- Signal Modes – Large Signals



Third signal chain

- Current > 20 mA
- TIA input saturates, ESD diodes open
- Voltage over diodes measured
- Combined input resistance $R \approx 5\ \Omega$



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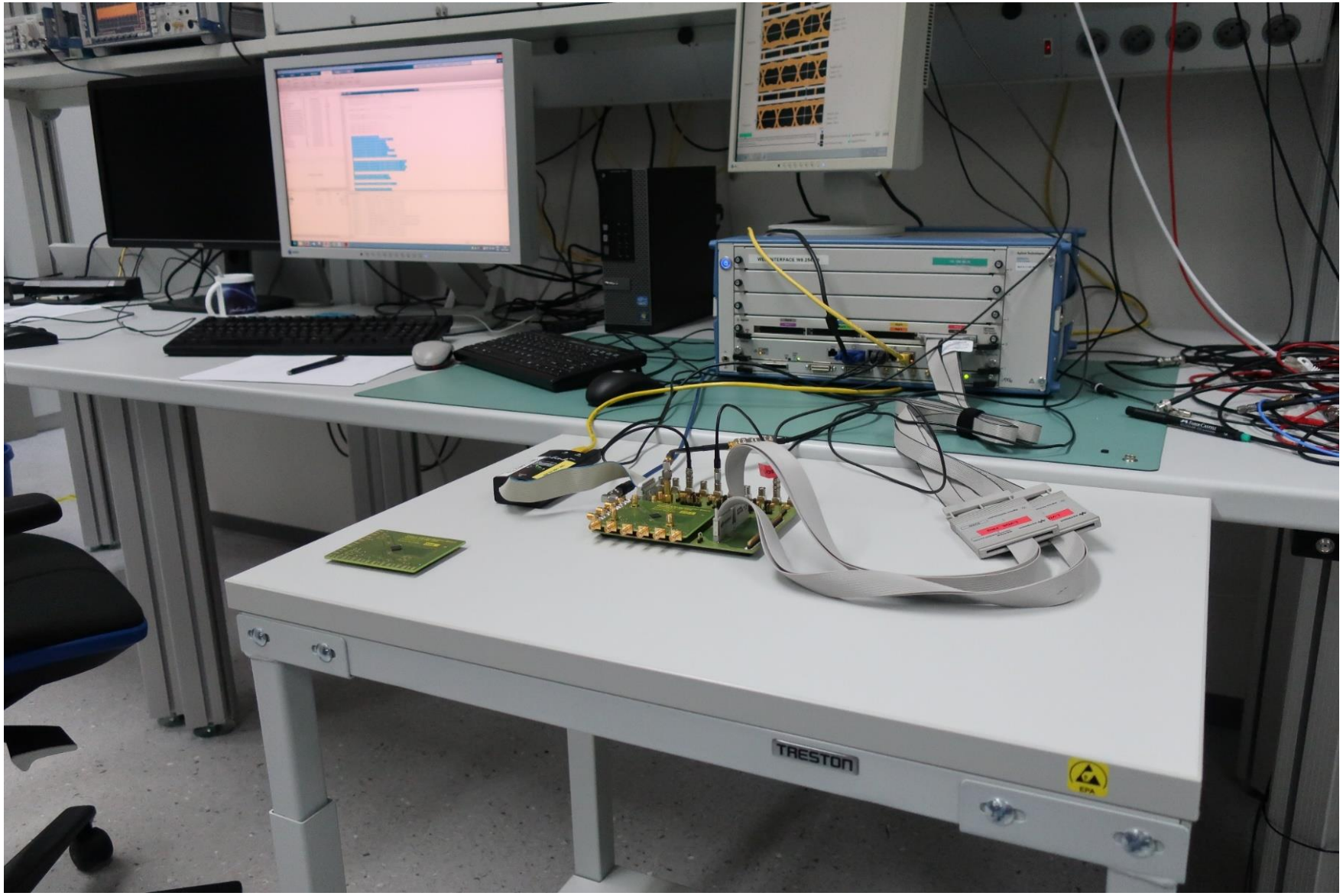

LAB SETUP OVERVIEW

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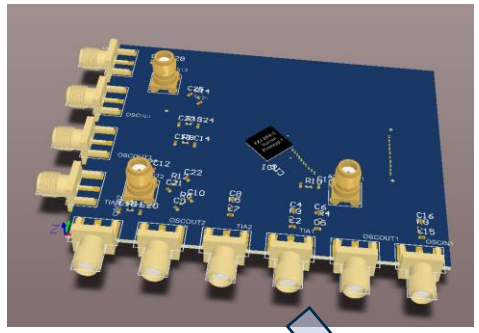
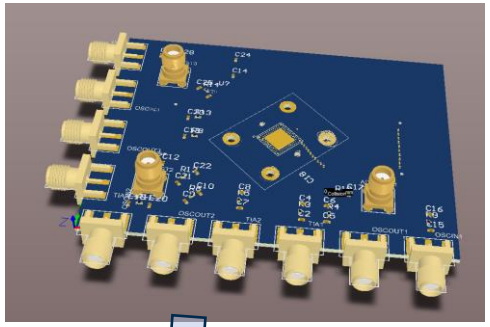
BOARD CONCEPT

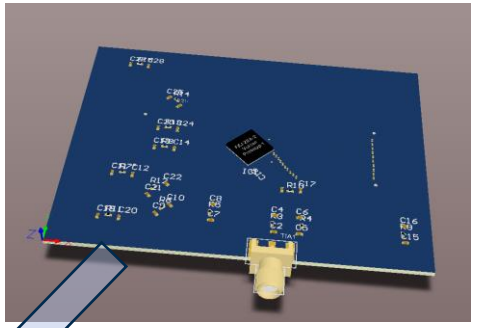
Verification Board
- Board for IC Verification
- Every ADC can be measured
- Best RF/Impedance performance
- Optimized for verification measuremens

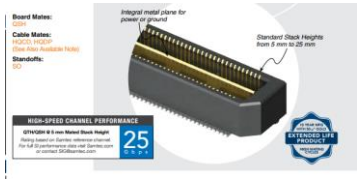


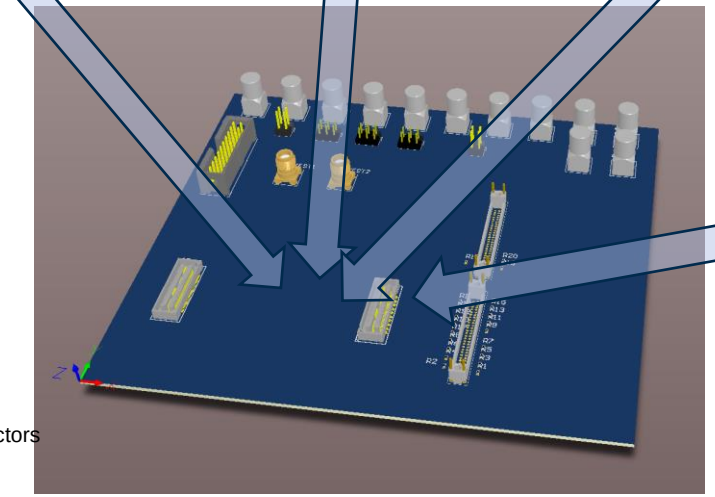
Socket Board
- Socket can be populated on board
- For measurement of many samples
- Limited performance measurements
- Functional checks



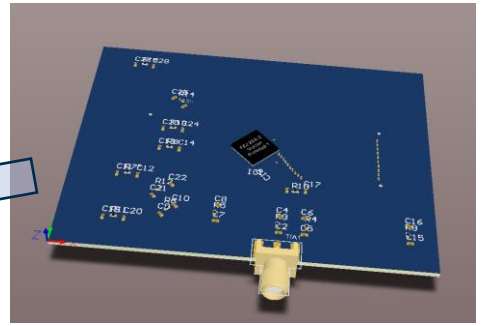
PMT Board
- For direct usage with PMT
- Protection circuit
- All 3 ADCs connected





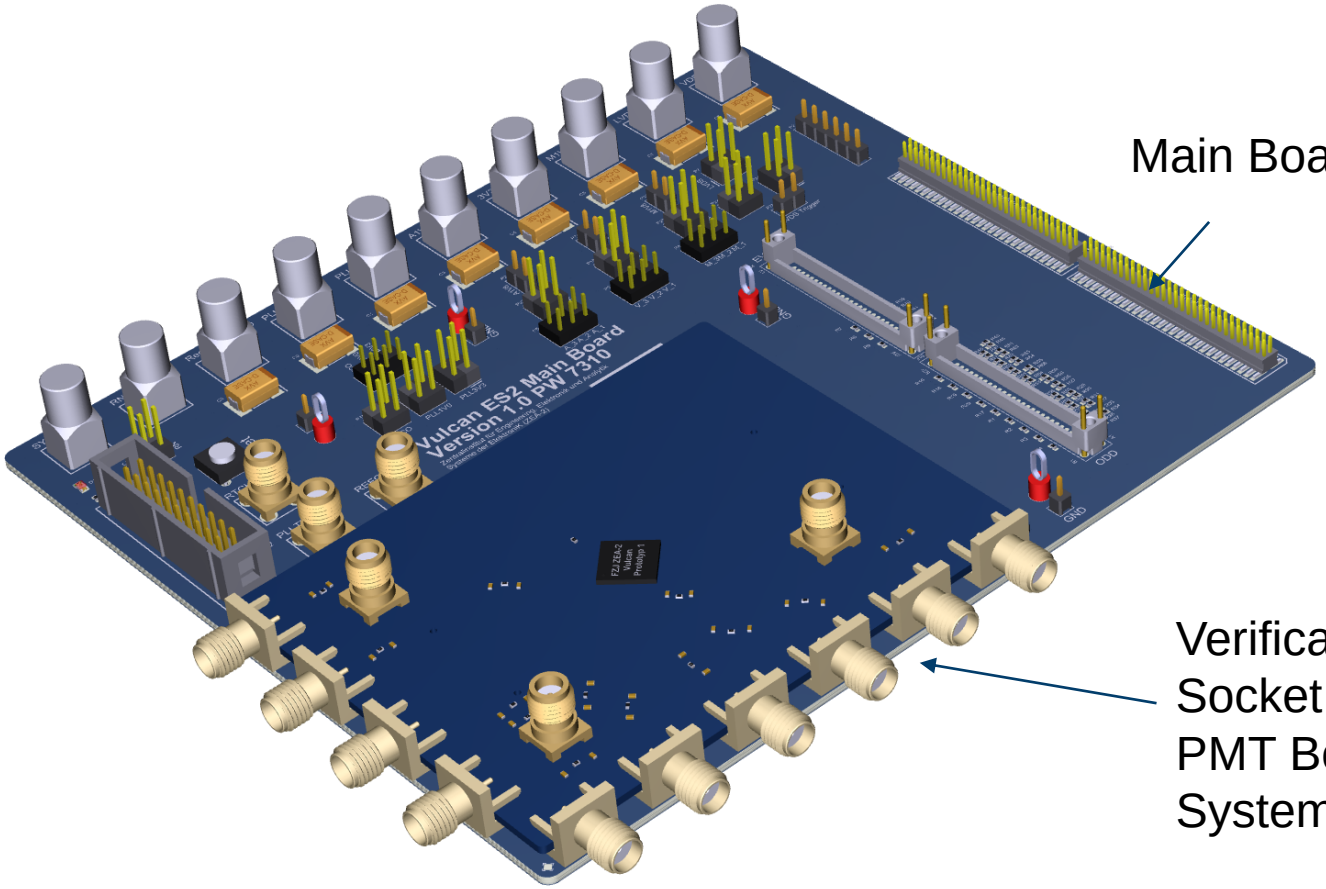


System Board
- All 3 ADCs connected
- Protection circuit
- Reference design for system implementation



Main Board
- Logic analyser connection
- Power supply connection
- JTAG interface
- DC measurements
- Samtec board to board connectors

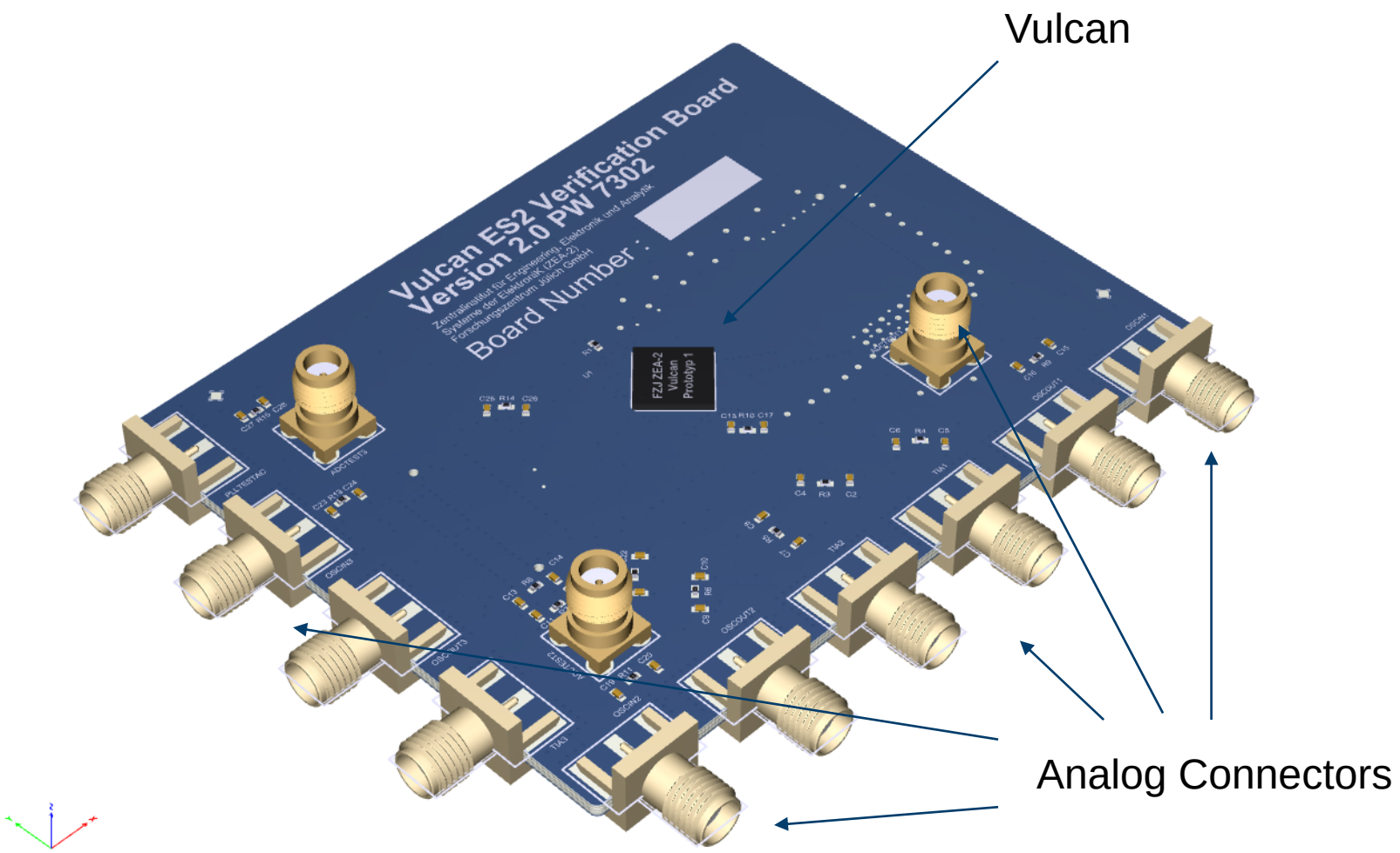
VERIFICATION BOARD CONCEPT



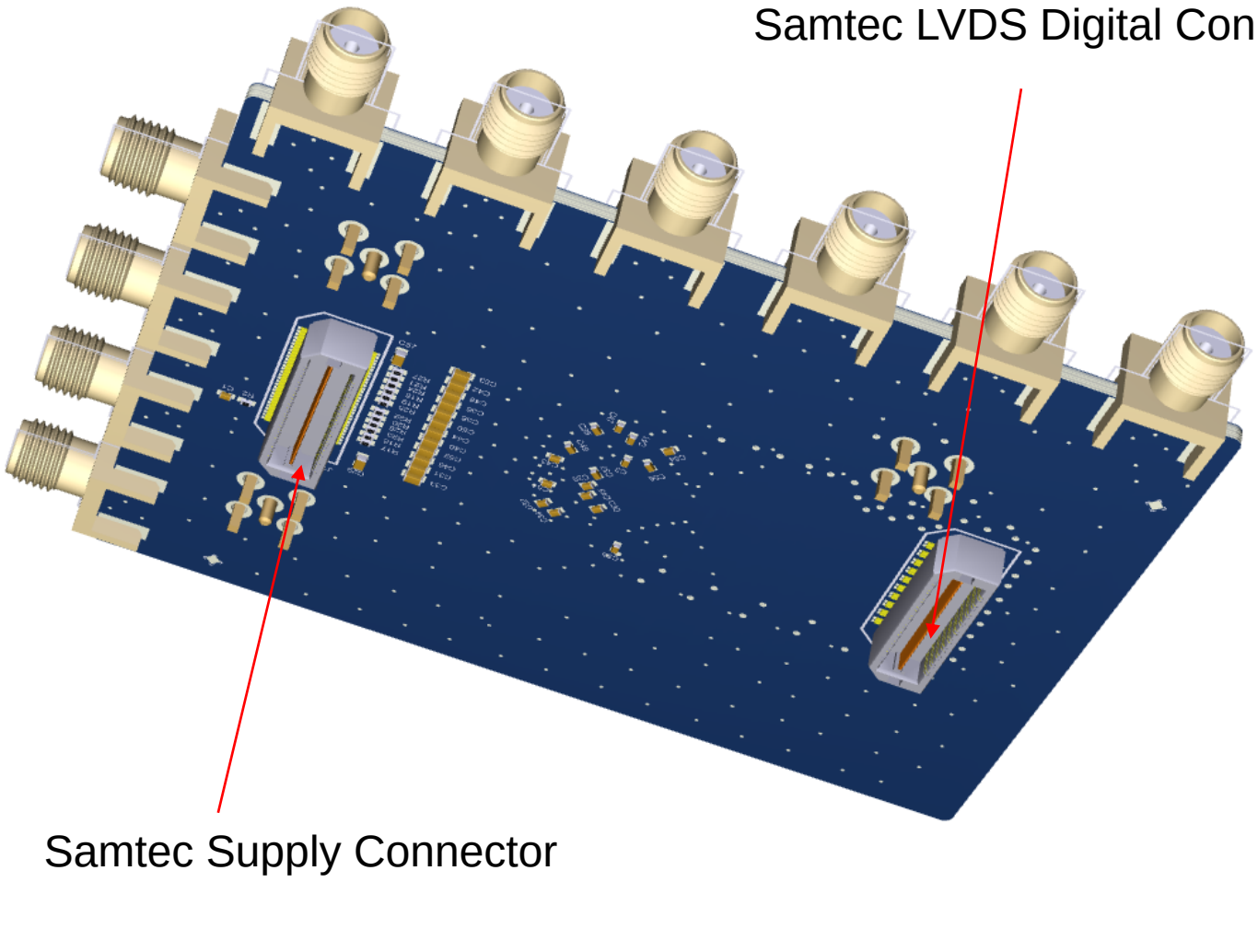
Main Board

Verification Board **or**
Socket Board **or**
PMT Board **or**
System Board

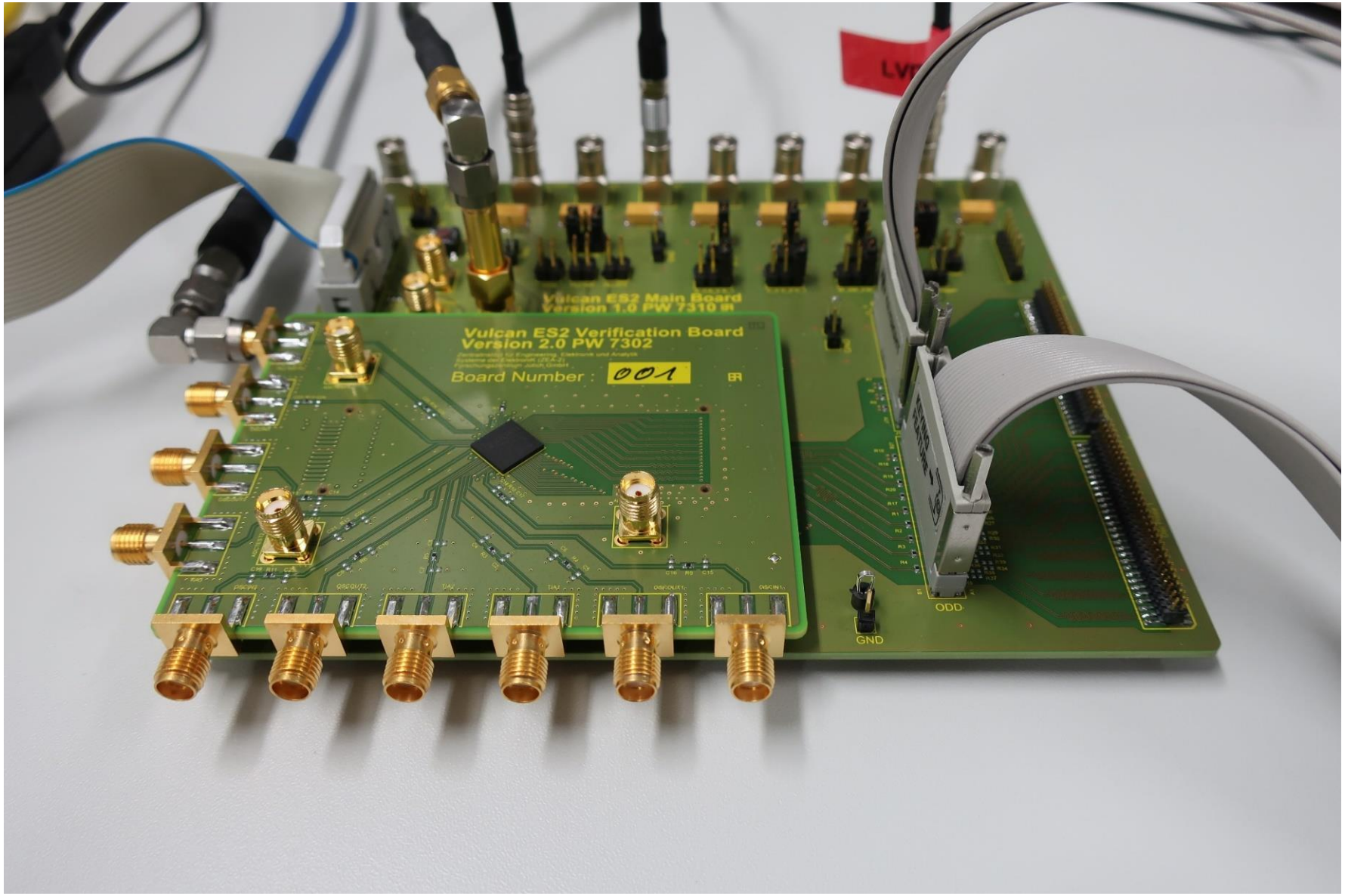
VERIFICATION BOARD



VERIFICATION BOARD

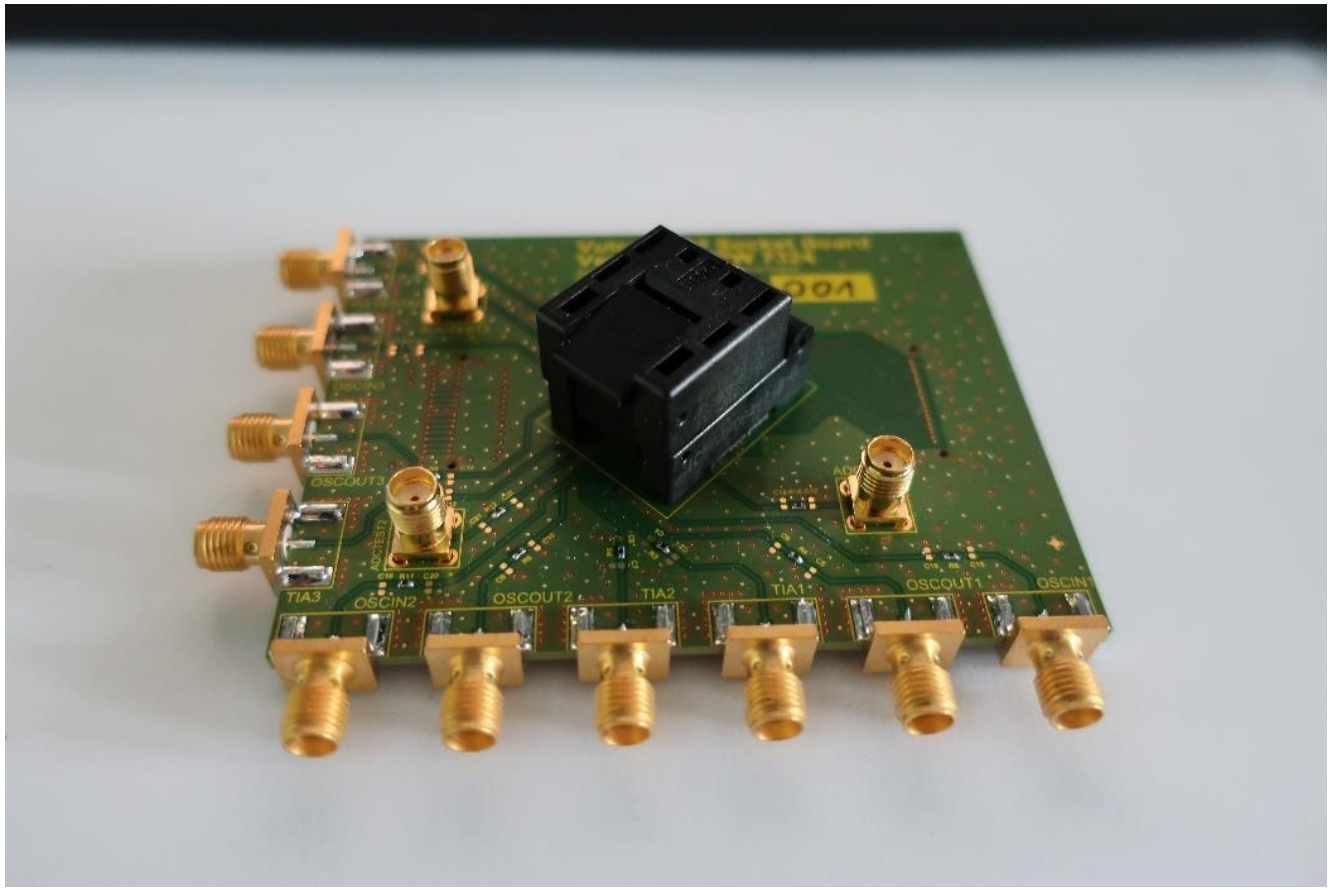


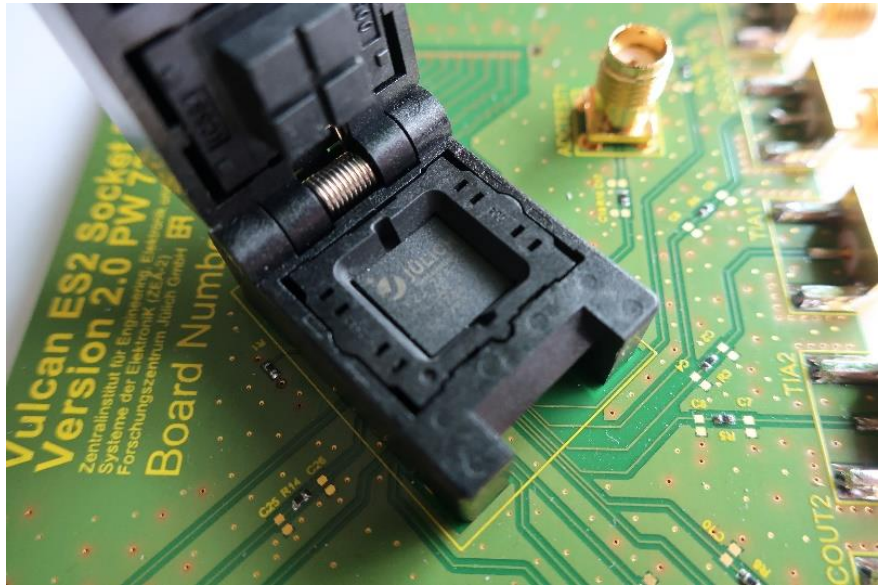
VERIFICATION BOARD SETUP

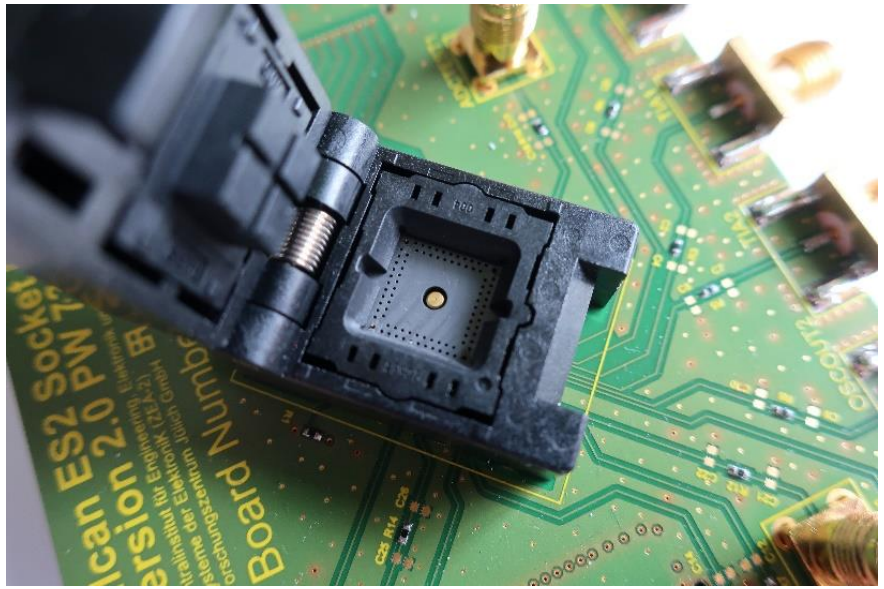


SOCKET BOARD SETUP

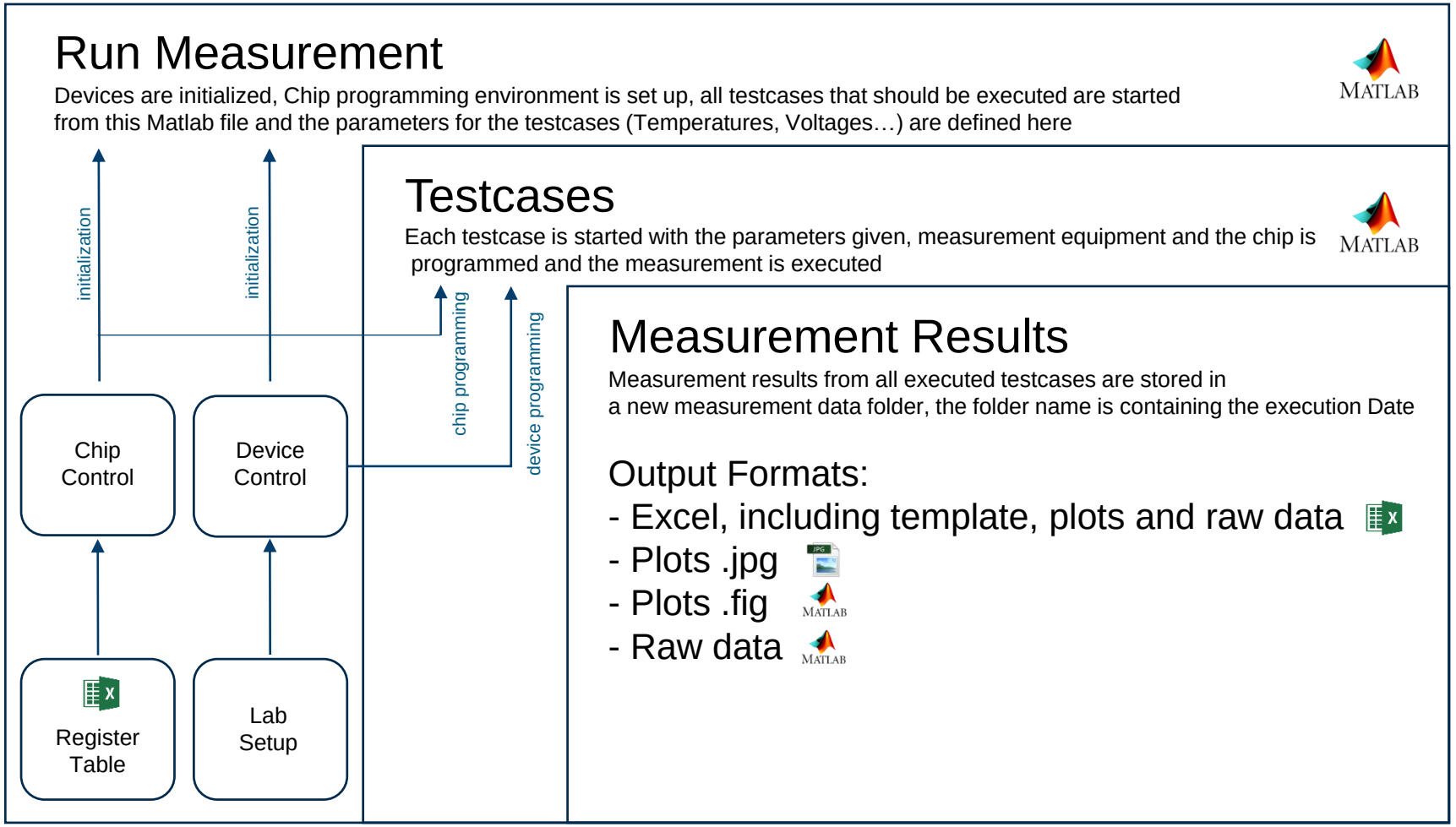
- Yamaichi Socket for functional testing





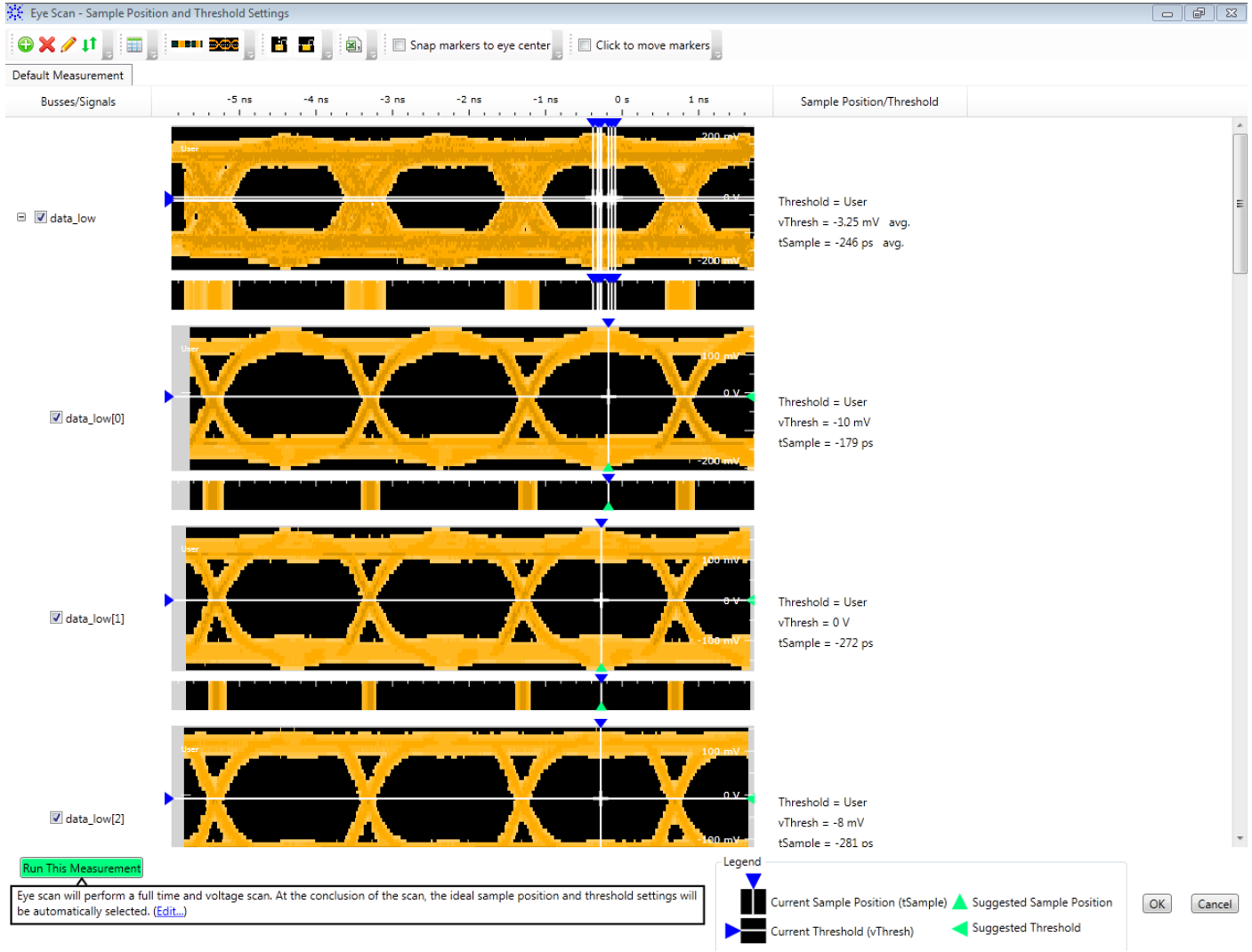


VERIFICATION SOFTWARE FRAMEWORK

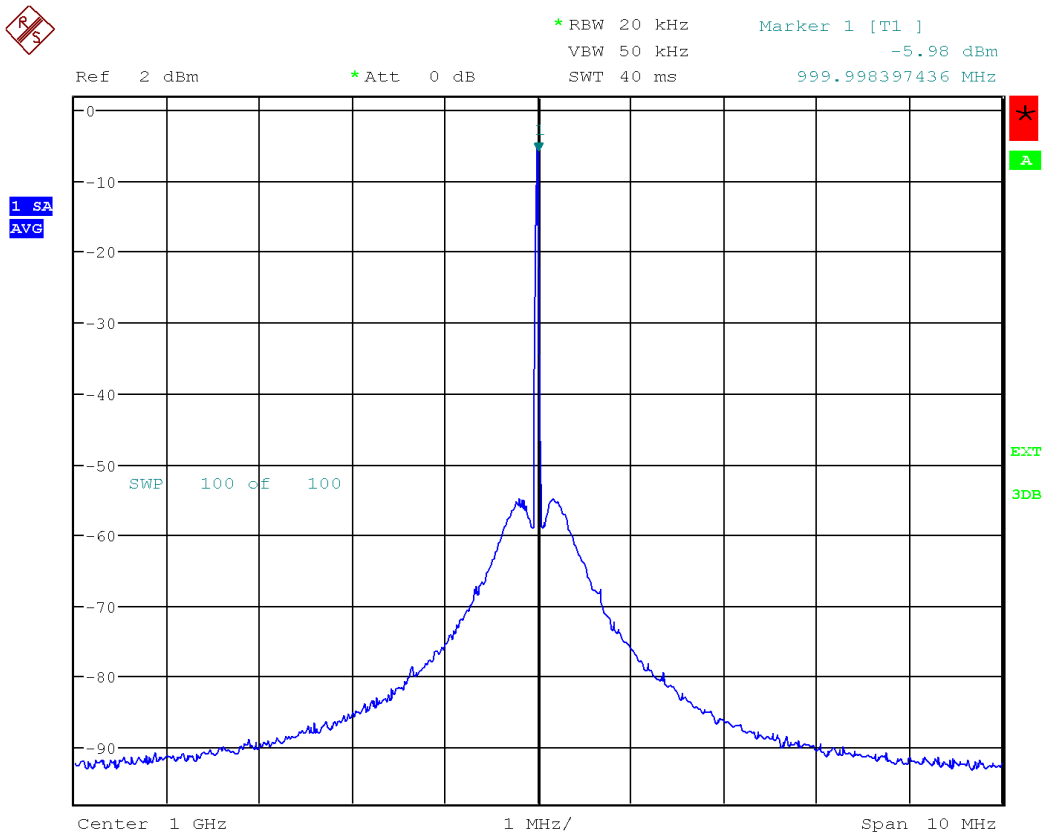


VERIFICATION RESULTS OF VULCAN ES2

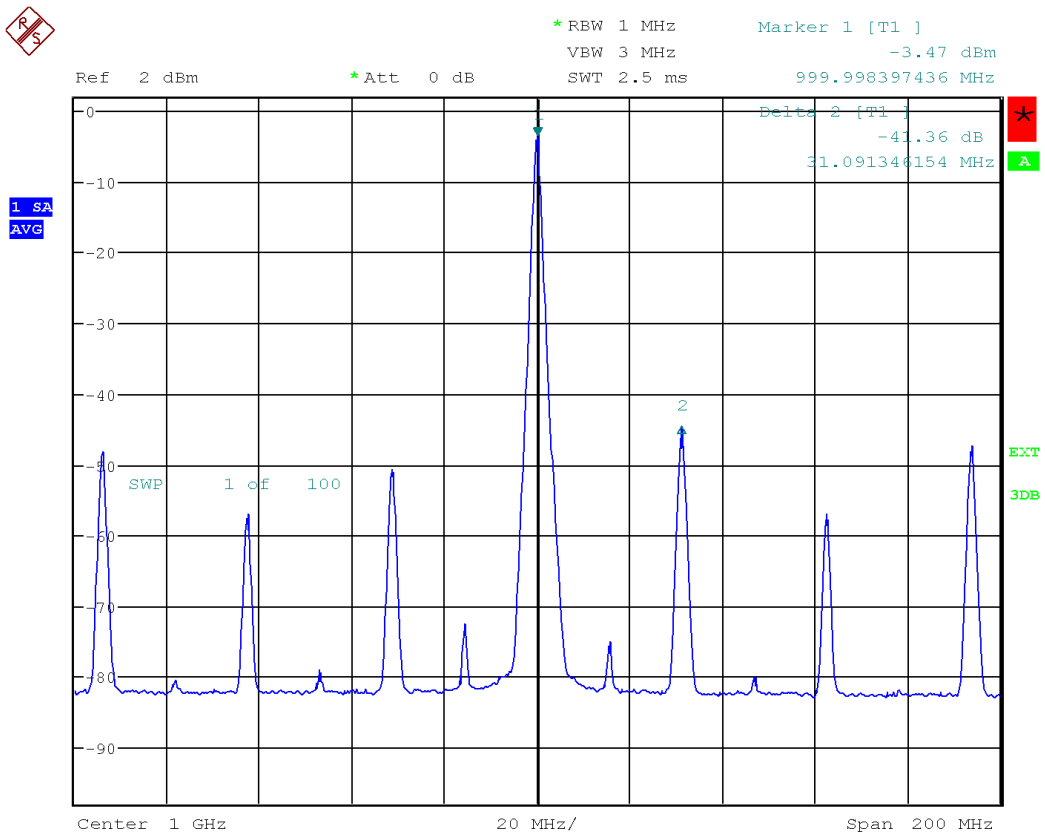
- LVDS Data Lines



VCO AND PLL INVESTIGATIONS



Date: 15.DEC.2003 07:15:24

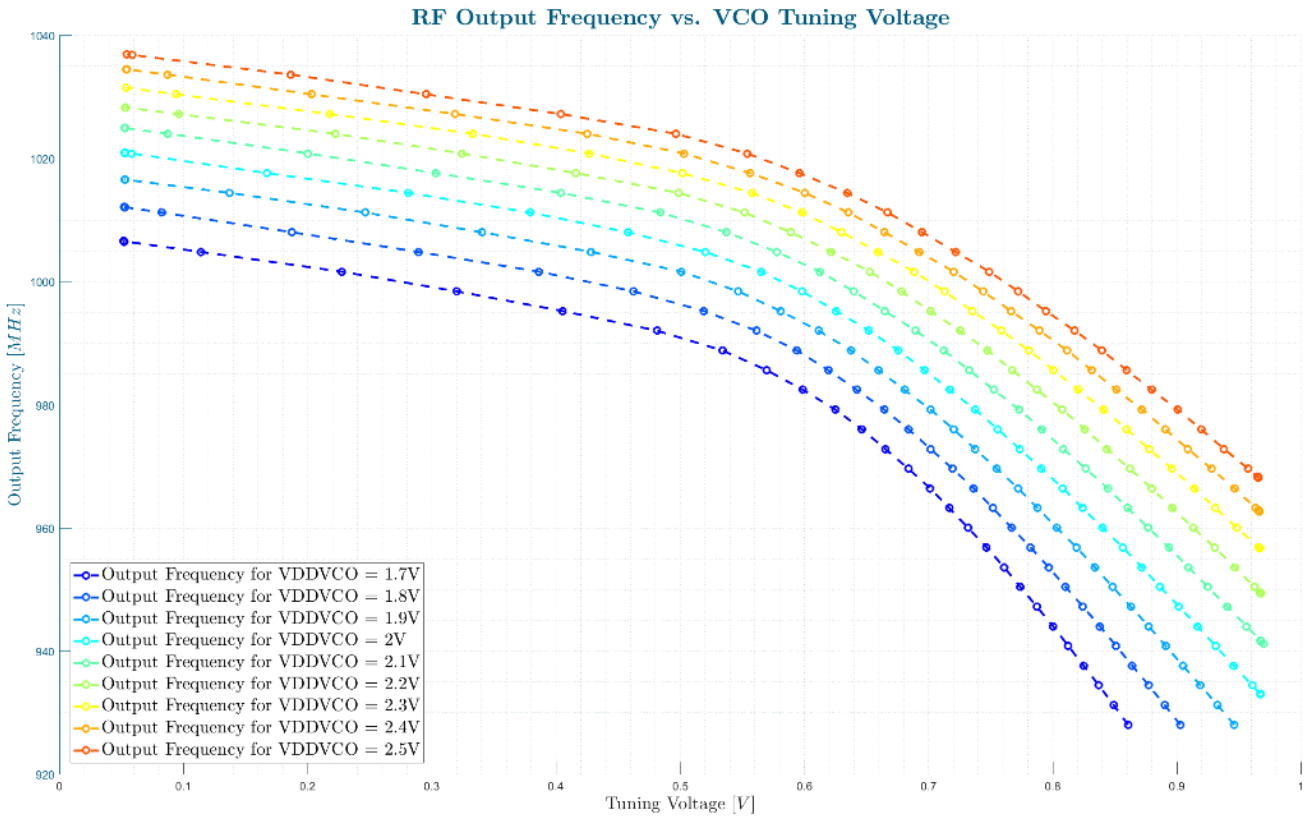


Date: 15.DEC.2003 07:17:58

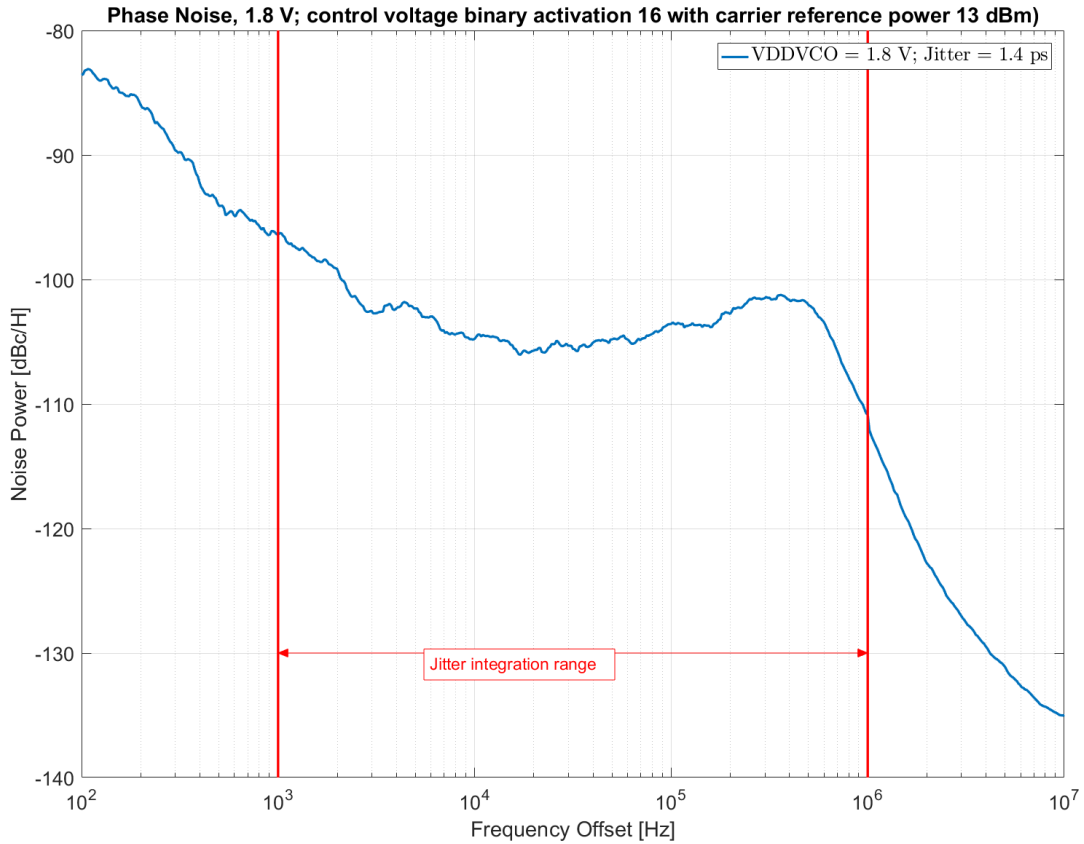
- VCO running @4GHz
- Reference clock for PLL @31.25MHz
- Measurement VCO/4 -> 1GHz

CLOCK AND PLL INVESTIGATIONS

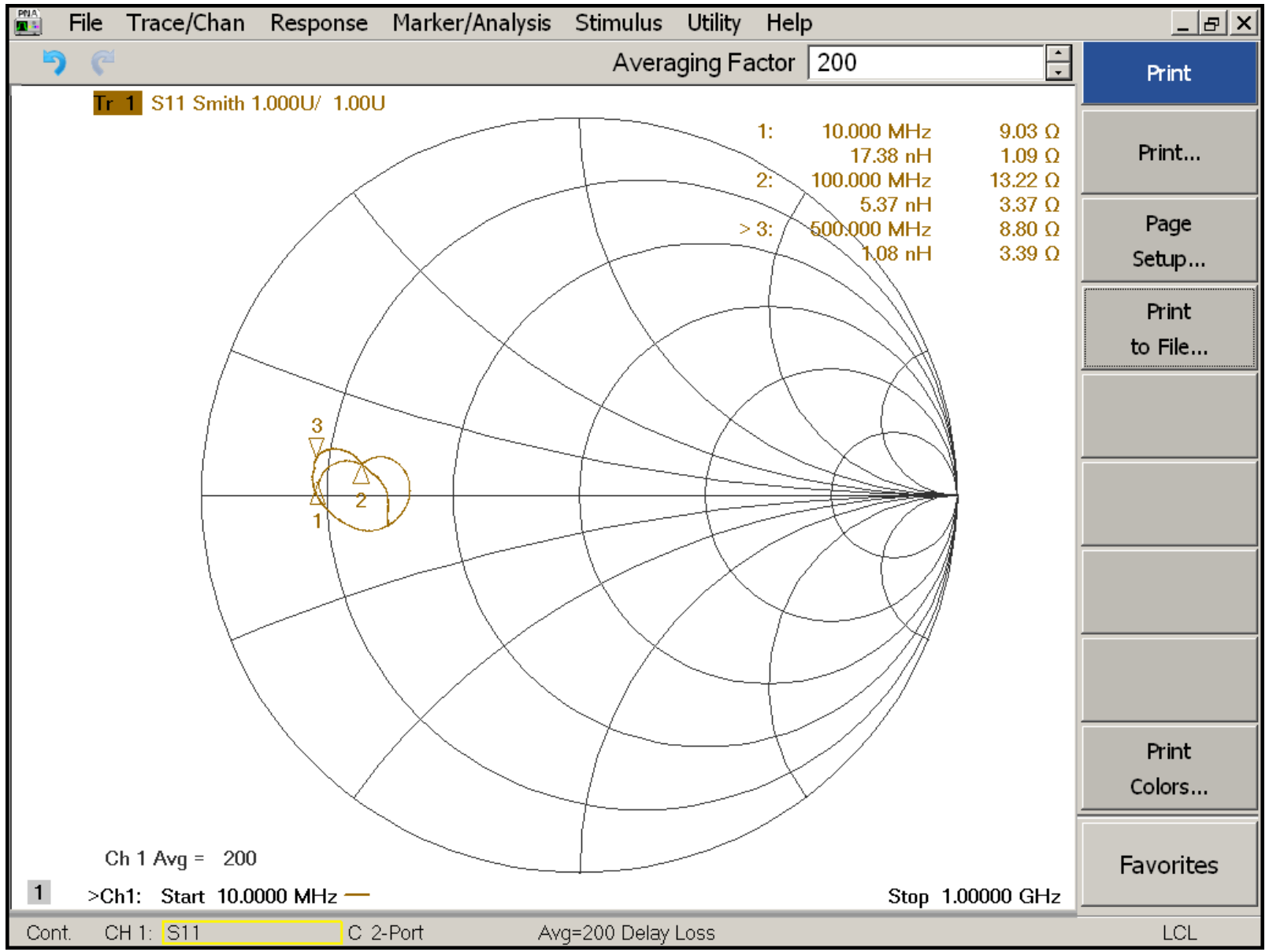
- VCO Tuning Range @ 25°C



- PLL Phase Noise @ 25°C



TRANSIMPEDANCE AMPLIFIER INPUT IMPEDANCE



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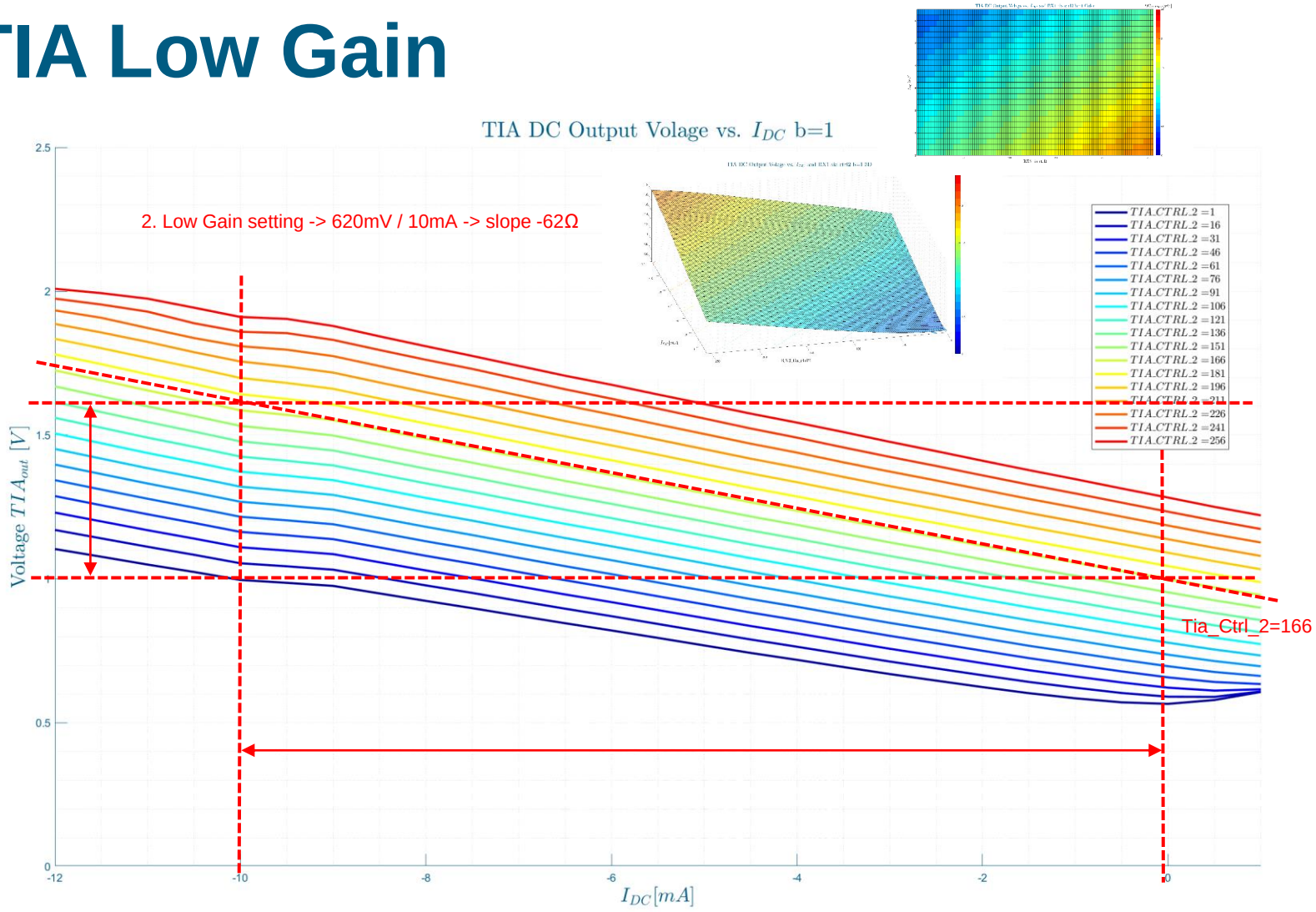
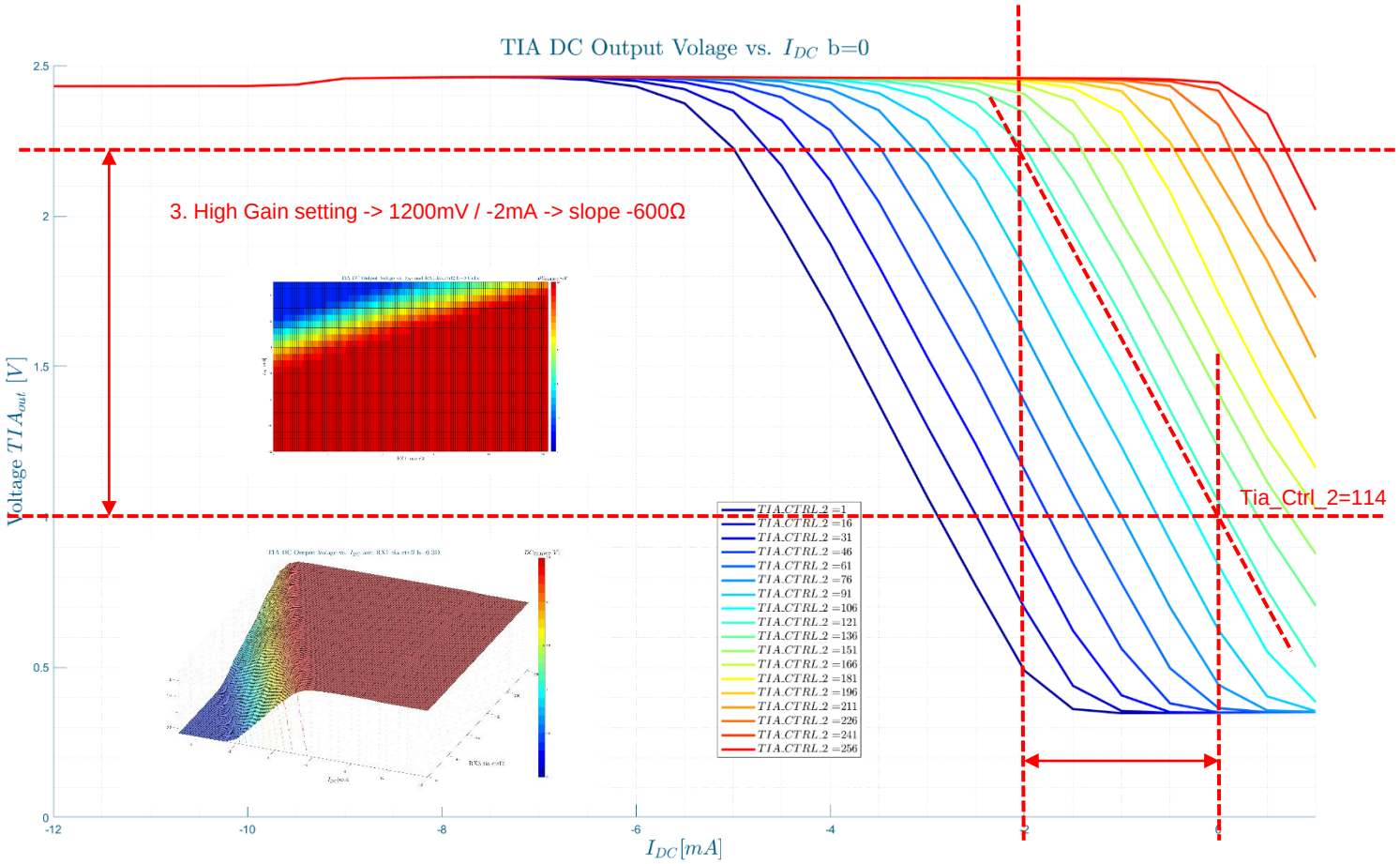
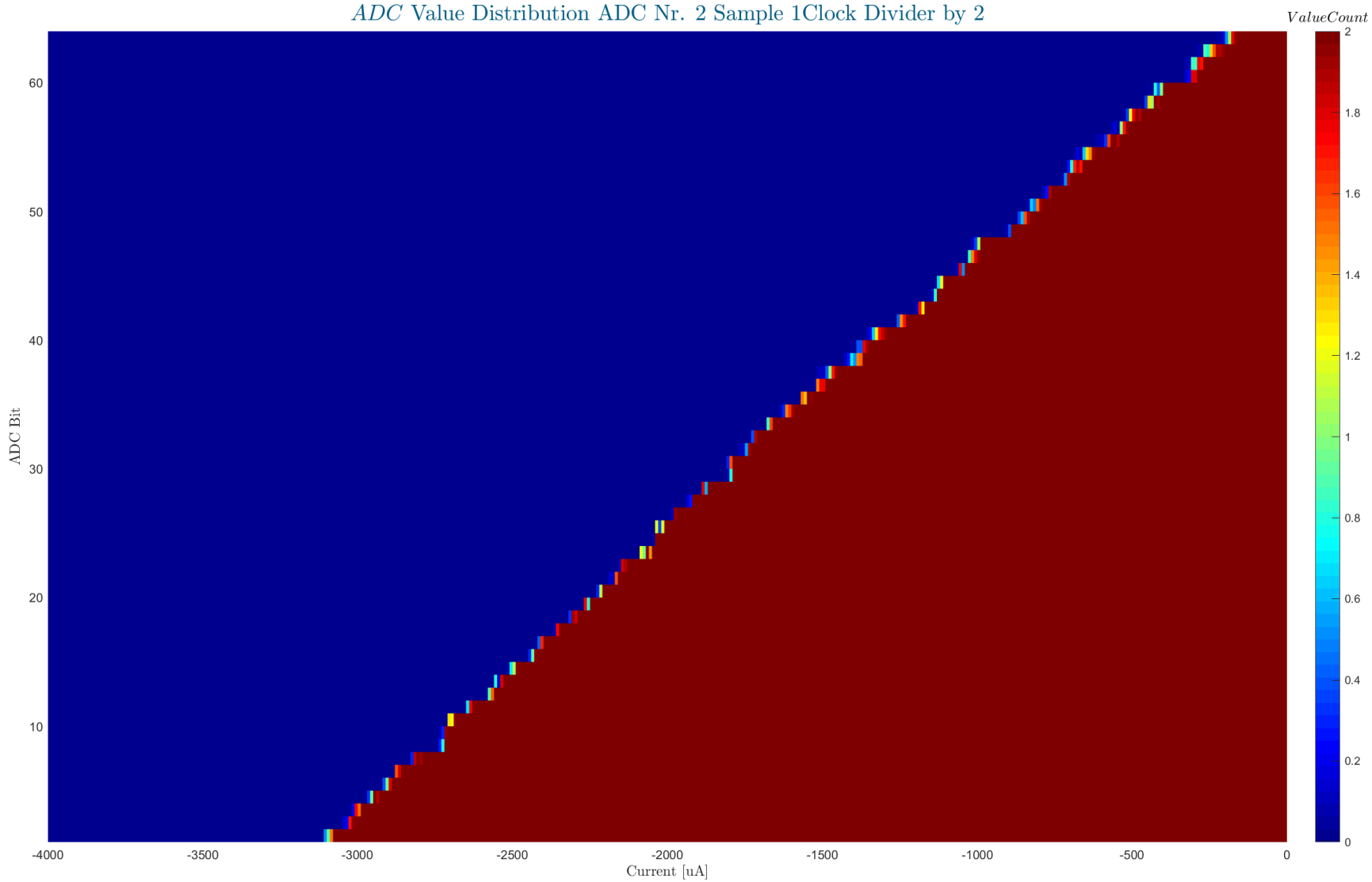
TIA Low Gain


TIA DC Output Volage vs. I_{DC} b=1
2. Low Gain setting -> 620mV / 10mA -> slope -62Ω
$TIA.CTRL\ 2 = 1$
$TIA.CTRL\ 2 = 16$
$TIA.CTRL\ 2 = 31$
$TIA.CTRL\ 2 = 46$
$TIA.CTRL\ 2 = 61$
$TIA.CTRL\ 2 = 76$
$TIA.CTRL\ 2 = 91$
$TIA.CTRL\ 2 = 106$
$TIA.CTRL\ 2 = 121$
$TIA.CTRL\ 2 = 136$
$TIA.CTRL\ 2 = 151$
$TIA.CTRL\ 2 = 166$
$TIA.CTRL\ 2 = 181$
$TIA.CTRL\ 2 = 196$
$TIA.CTRL\ 2 = 211$
$TIA.CTRL\ 2 = 226$
$TIA.CTRL\ 2 = 241$
$TIA.CTRL\ 2 = 256$
Tia_Ctrl_2=166
Voltage TIA_{out} [V]
$I_{DC}[mA]$
2.5
2
1.5
1
0.5
0
-12
-10
-8
-6
-4
-2
0

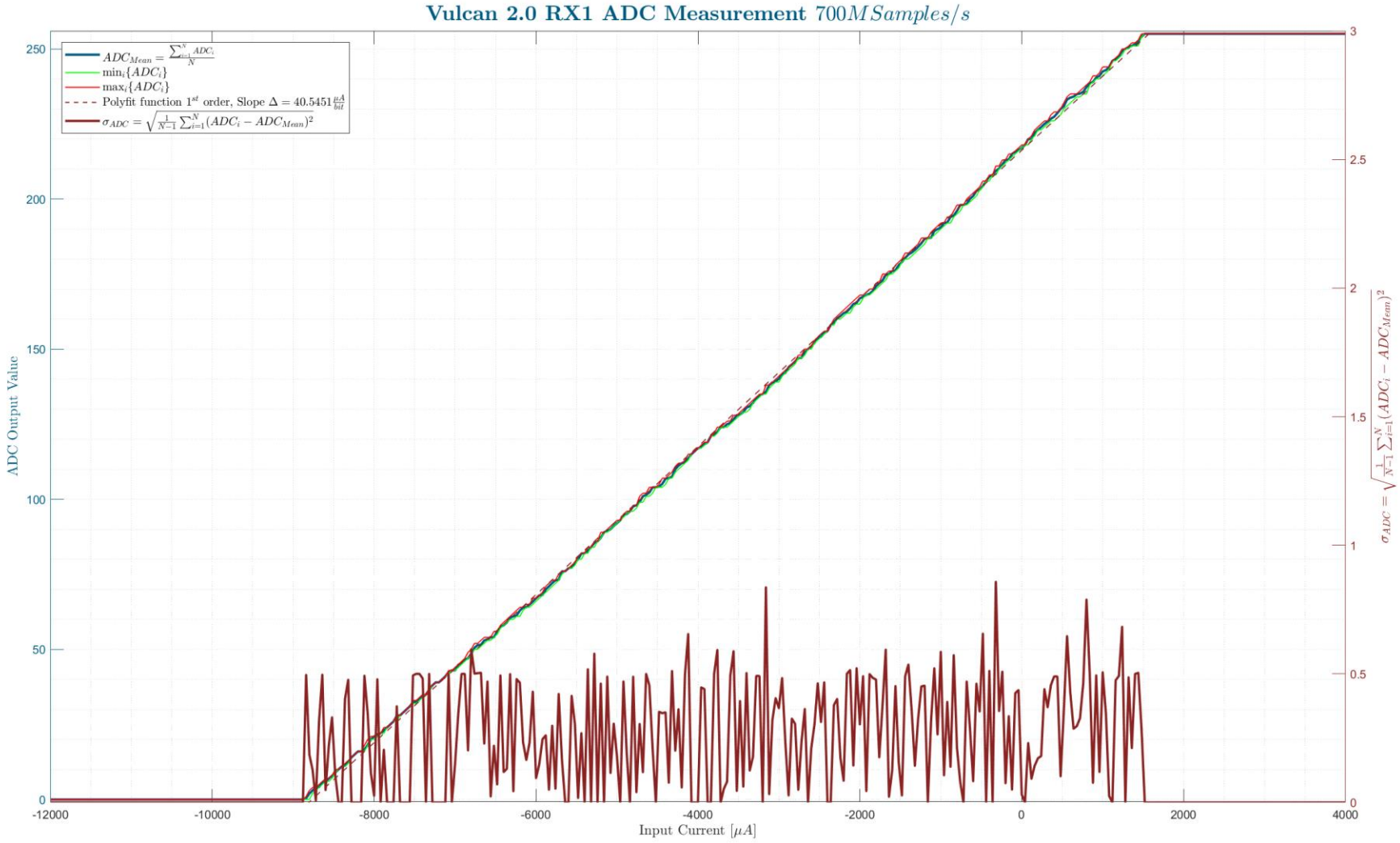
TIA High Gain



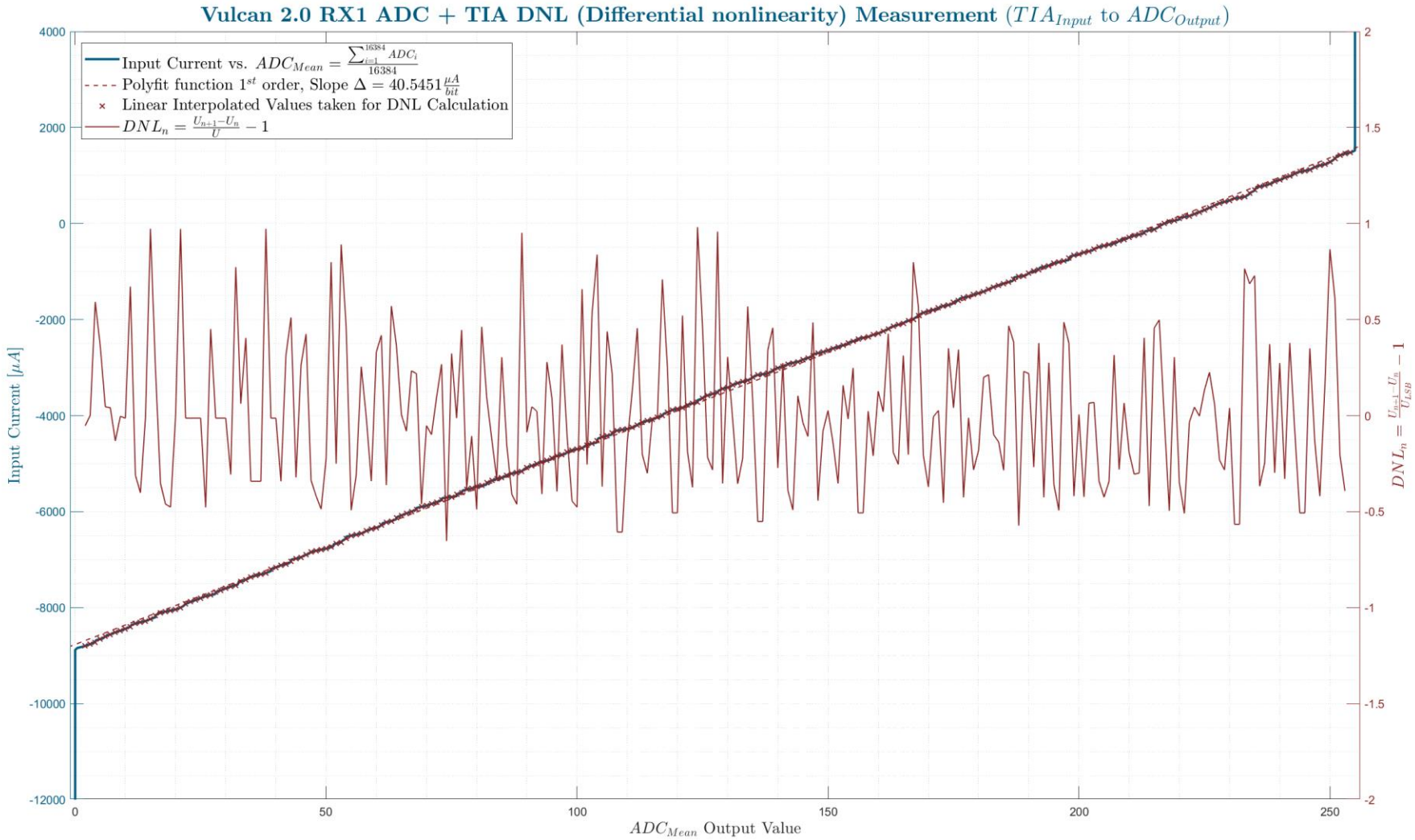
ADC Thermometer Code Distribution 500Msample/s



Full Range ADC Characteristic (low Gain)



Full Range ADC DNL (low Gain)



Scientific Challenges SCIENCE Electronic ZEA-2 Systems Applications and Methods

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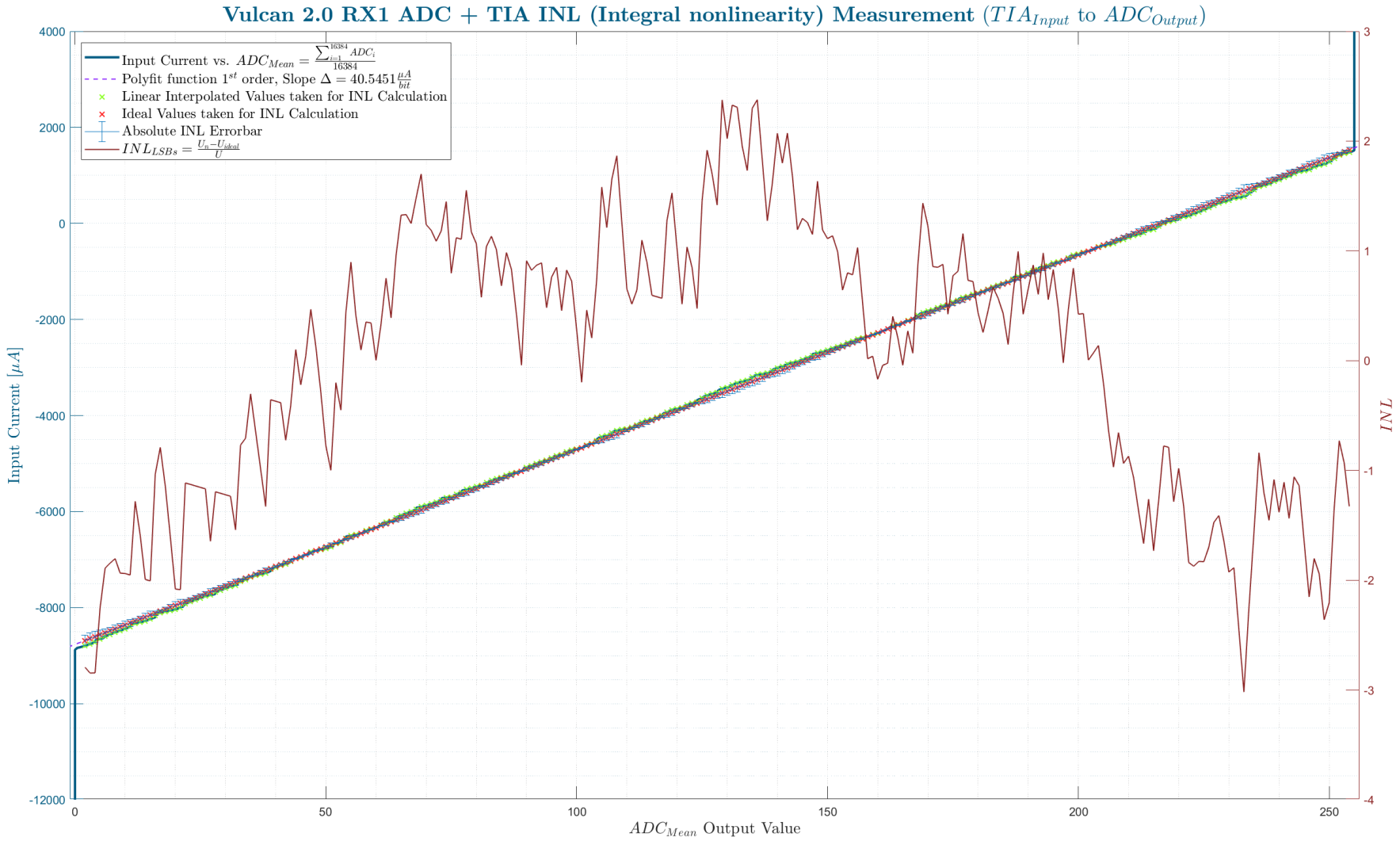
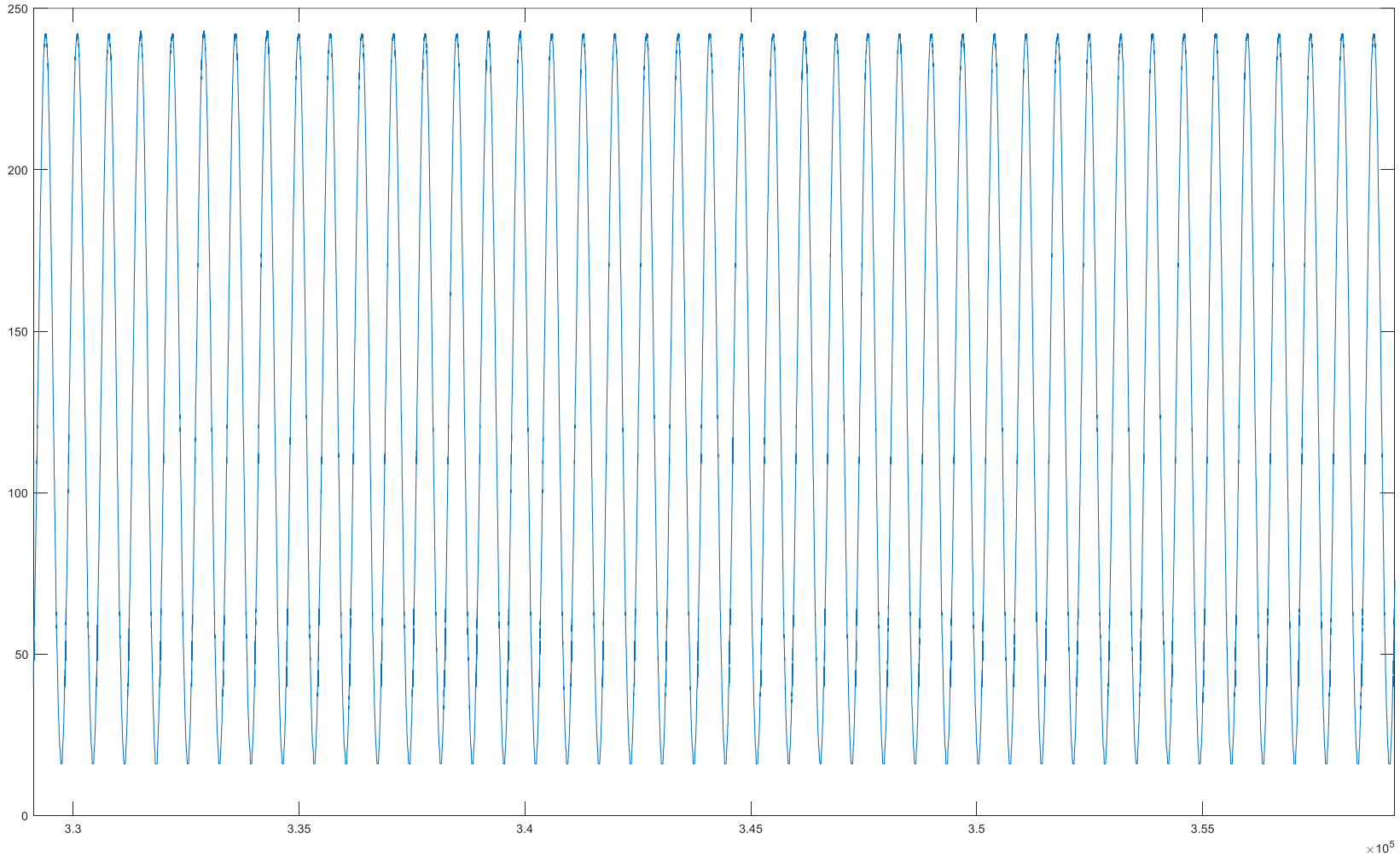
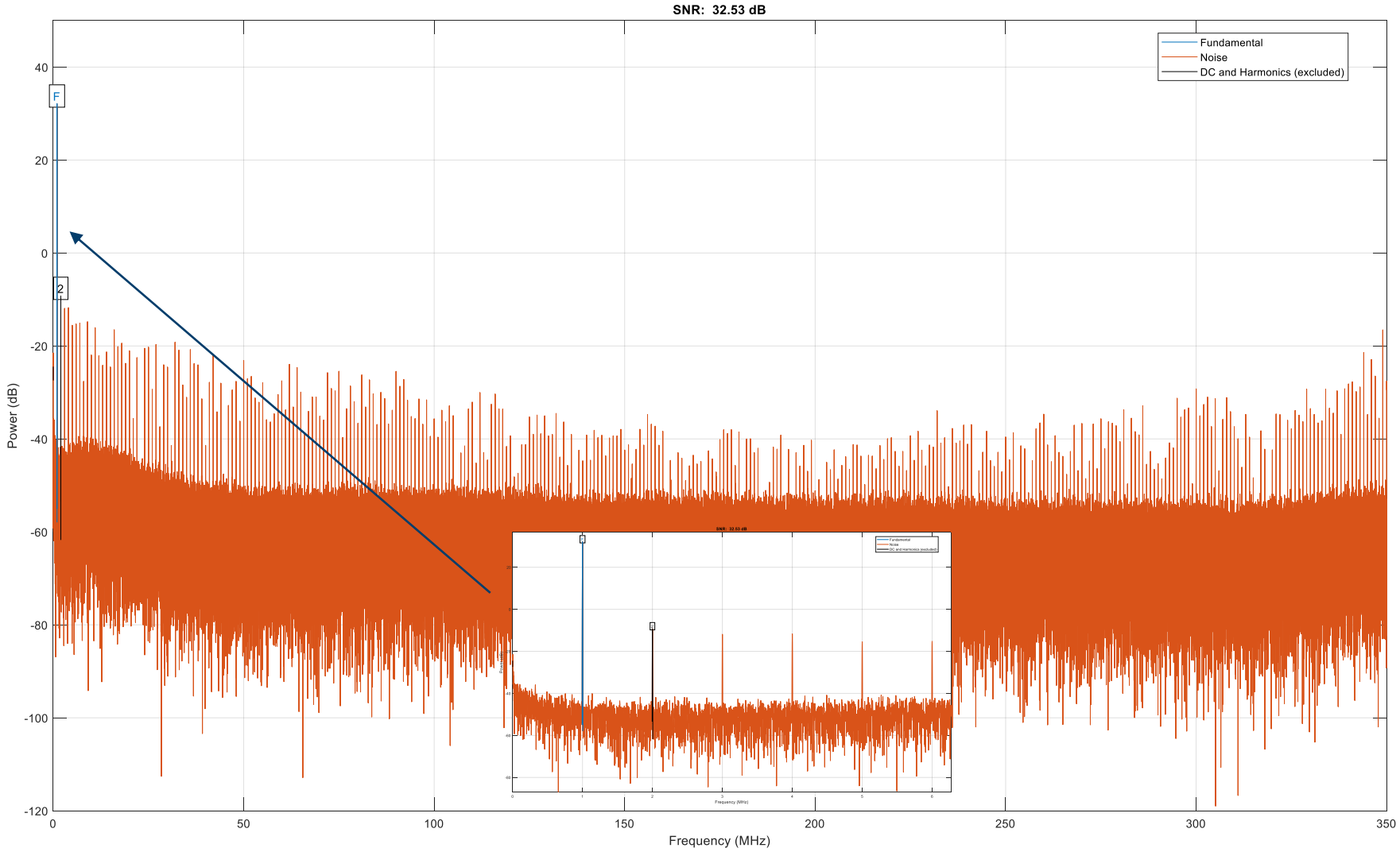
Full Range ADC INL (low Gain)



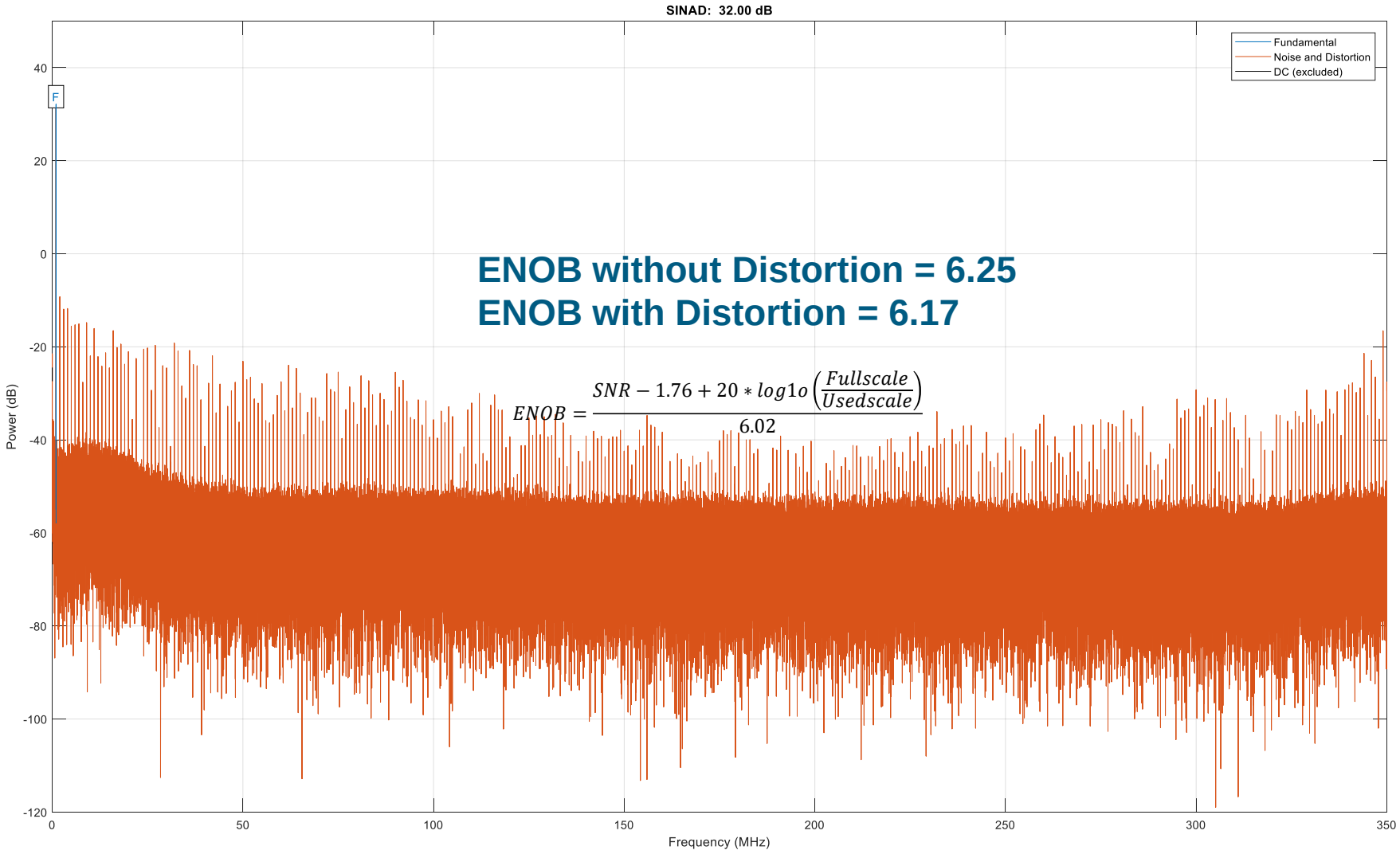
Sinewave Signal 1 MHz (700Msamples/s)



SNR Measurement (700Msamples/s)



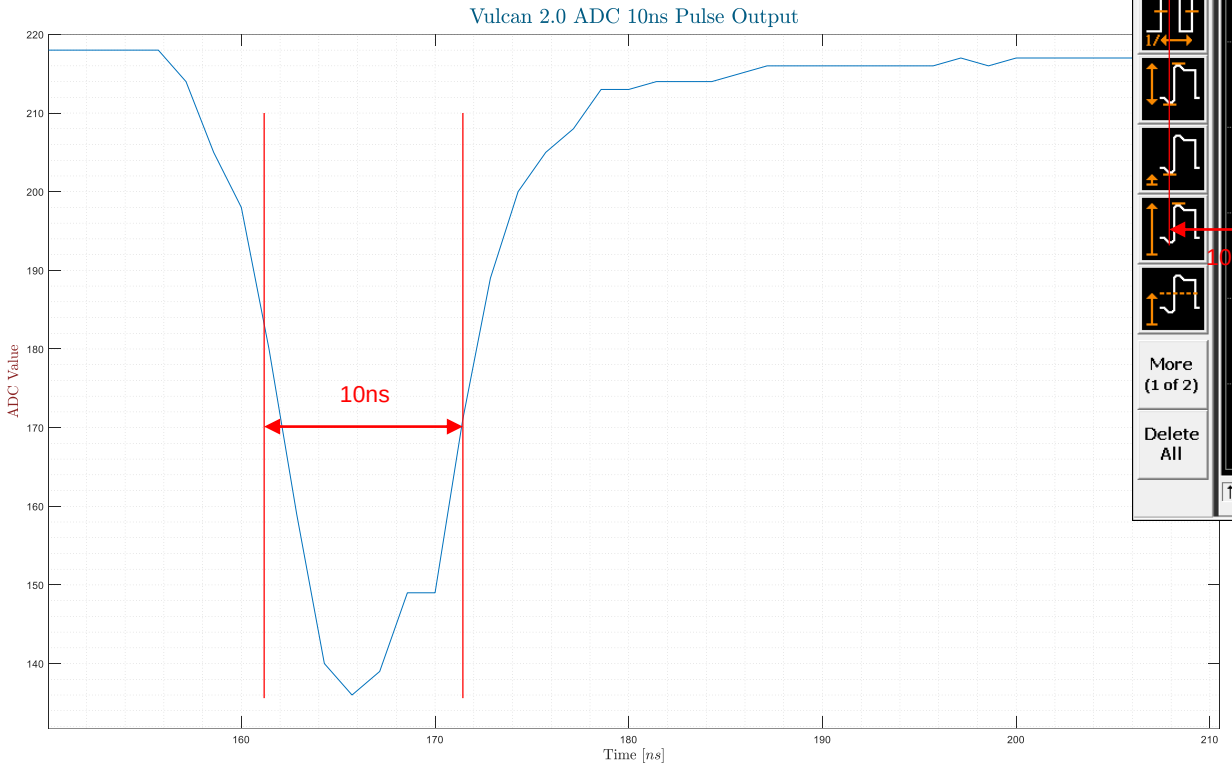
SNR Measurement with Distortion (700MSamples/s)

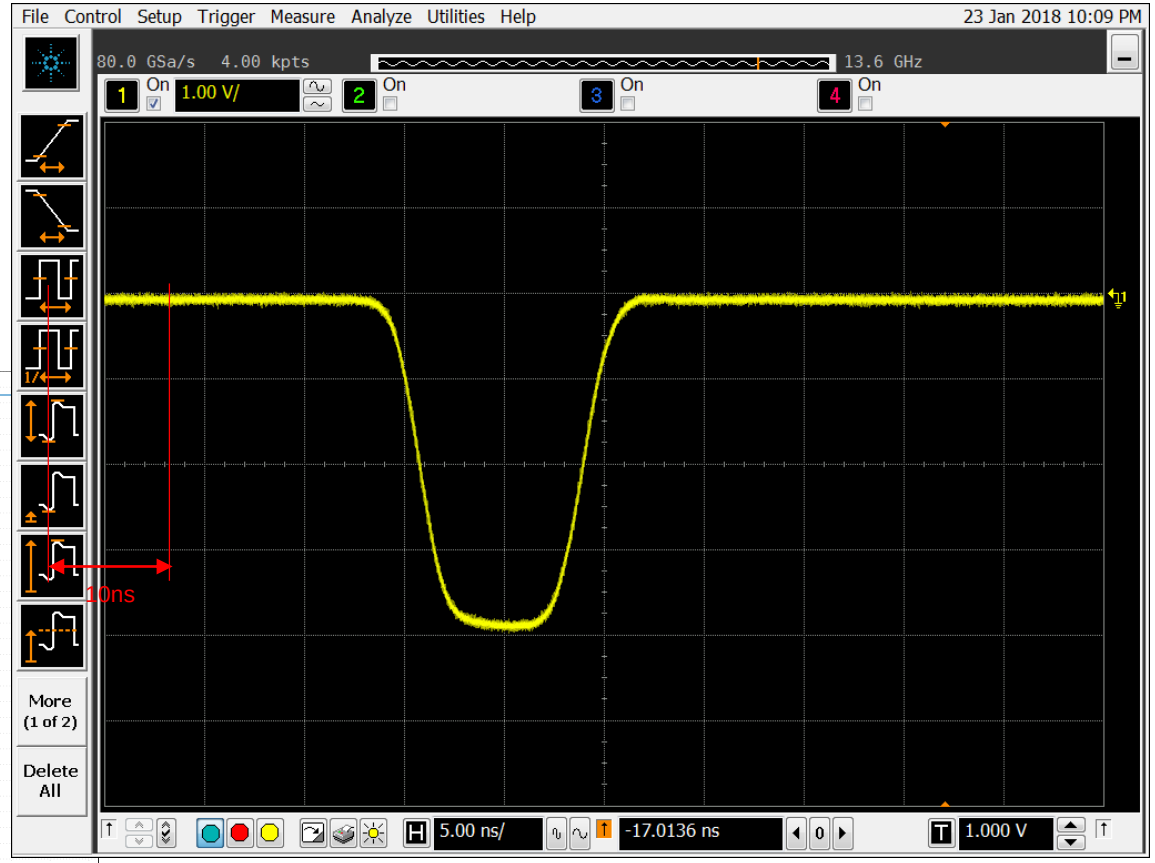


ENOB without Distortion = 6.25
ENOB with Distortion = 6.17

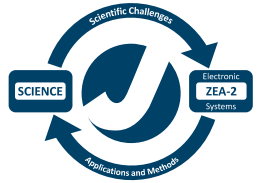
$$ENOB = \frac{SNR - 1.76 + 20 * log1o\left(\frac{Fullscale}{Usedscale}\right)}{6.02}$$

10ns Pulse ADC Output





Vielen Dank!


Scientific Challenges
SCIENCE
Electronic
ZEA-2
Systems
Applications and Methods